IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chi, et al.	Docket No.:	TSM03-0422
Serial No.:	10/718,920	Art Unit:	TBD
Filed:	November 21, 2003	Examiner:	TBD
For:	Modification of Carrier Mobility in a Semiconductor Device		

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Date of Deposit: March 11, 2004

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Information Disclosure Statement (1 page)
IDS Form PTO/SB/08a and 08b (2 pages) citing (10) references
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Respectfully submitted,

Natalie Swider

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a & 08b that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

March 11, 2004
Date

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PTO/SB/08a (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	2

Complete if Known	
Application Number	10/718,920
Filing Date	11/21/2003
First Named Inventor	Chi, et al.
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	TSM03-0422

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2003/0162348 A1	08-28-2003	Yeo, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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Sheet 2 of 2

Complete if Known	
Application Number	10/718,920
Filing Date	11/21/2003
First Named Inventor	Chi, et al.
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	TSM03-0422

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	2	Rim, K., et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," IEEE Transactions on Electron Devices, vol. 47, no. 7, pp. 1406-1415, July 2000.	
	3	Rim, K., "Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology," IEEE International Solid-State Circuits Conference, paper #7.3, pp. 116-117, 2001.	
	4	Yeo, Y.C., et al., "Enhanced performance in Sub-100 nm CMOSFETs using Strained Epitaxial Silicon-Germanium," International Electron Device Meetings, pp. 753-756, 2000.	
	5	Ootsuka, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meetings, pp. 575-578, 2000.	
	6	Ito, S., et al., "Mechanical Stress Effect of Etch-Stop Nitride and Its Impact on Deep Submicron Transistor Design," International Electron Device Meetings, pp. 247-250, 2000.	
	7	Shimizu, A., et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," International Electron Device Meetings, pp. 433-436, 2001.	
	8	Ota, K., et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," International Electron Device Meetings, pp. 27-30, 2002.	
	9	Scott, G., et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress," International Electron Device Meetings, pp. 827-830, 1999.	
	10	Bianchi, R.A., et al., "Accurate Modeling of Trench Isolation Induced Mechanical Stress Effects on MOSFET Electrical Performance," International Electron Device Meetings, pp. 117-120, 2002.	

Examiner Signature		Date Considered	

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